Session 23 Overview

Technology and Architecture Directions

Chair: Werner Weber, Infineon, Munich, Germany

Associate Chair: C-K Wang, National Taiwan University, Taipei, Taiwan

New technology and architecture solutions have the potential to enable exciting and powerful applications. This session introduces several such applications with improved power, energy, and/or performance.

Paper 23.1 demonstrates the generation of 1μW of electrical power from 1 milliCurie of benign Nickel-63 nuclear energy source at over 30% conversion efficiency. Such an energy source has the potential to enable self-powered sensor networks. Measurements show that the energy source can provide about 20nW of continuous power for low-power sensors or up to 40μW of peak power for burst mode computation and communication.

The second paper presents the first comprehensive comparison of digital and analog building blocks in FinFET and Triple-Gate transistor technologies. These multi-gate transistor technologies offer the promise to continue Moore's law of scaling by improving device electrostatics. Ring oscillator modules comprised of various CMOS logic gates, frequency dividers, and operational amplifiers demonstrate the highest level of integration reported to date using these multi-gate devices.

Paper 23.3 presents a low-power low-cost random number generator for embedded security systems. Random number generation is achieved by using the noise due to oxide traps of small area MOSFETs. This concept of random number generation is robust against external process, voltage, and temperature variations.

Papers 23.4 and 23.5 demonstrate fast yet energy efficient data communication concepts. Paper 23.4 introduces high data rate communication between chips that are three-dimensionally stacked without the need for expensive through-silicon vias. The communication between three-dimensionally stacked chips is achieved with inductive coupling. While occupying only 2mm^2, the chips have 1024 data transceivers with a data rate of 1Gb/s per channel. The high density is achieved by using 4-phase time division multiplexing to reduce cross-talk resulting in a negligible bit error rate. The energy efficiency of the communication is 3pJ/b. The resulting solution provides an aggregate data rate of 1Tb/s and consumes 3W. Paper 23.5 introduces a new approach for realizing high-speed optical interconnects on silicon chips. This concept uses nano-photodiodes on silicon with extremely low parasitic capacitance (less than 10aF) enabling robust communication at very high frequencies. The results demonstrate 5GHz clocking with the promise of up to 20GHz. The authors will also discuss how the silicon nano-photodiode can be used for wavelength-division multiplexing and low-voltage electro-optic modulators for on-chip and off-chip optical communications.

Novel low-power architectures for computation and communication are presented in the next two papers. In Paper 23.6, the authors present the first single-chip globally-asynchronous locally-synchronous reconfigurable processor for DSP applications. The 475MHz reconfigurable processor has been tested for JPEG encoding and 802.11a/g transmitter applications. In Paper 23.7, the authors present a system-in-silicon architecture with 1024b inter-chip bus to provide high-bandwidth low-power connectivity between logic and memory. The highly parallel architecture also allows low frequency (25MHz) operation while achieving real-time motion estimation for 1080HDTV. The solution achieves the required 23.1Gb/s bandwidth and associated processing for motion estimation at a power level of 190mW.

The final paper in this session introduces the first chip-scale soliton modelocked oscillator in CMOS. The pulse width is reduced by 10X compared to previous non-integrated modelocked oscillators. It is expected that this research will lead to pulse widths as short as 1ps.

23.1 Active Circuits for Ultra-High-Efficiency Micropower Generators Using Nickel-63 Radioisotope **8:30 AM**
R. Duggirala, Cornell University, Ithaca, NY

Integration of betavoltiacs with radioisotope-powered piezoelectric micropower generators (RPG) operating in new *resonant* modes, attains nuclear-electrical conversion efficiencies of up to 30%, generating 1 to 10μW peak power with 1 to 10 milliCurie of Nickel-63. A 20mV-voltage-drop ac-to-dc rectifier employing radioactively biased MOSFETs is developed for efficient conversion of RPG-generated low-amplitude power signals.

23.2 Circuit Design Issues in Multi-Gate FET CMOS Technologies **9:00 AM**
C. Pacha, Infineon, Munich, Germany

Multi-gate FETs are promising for sub-45nm CMOS technologies. To address the link between design and technology, basic digital and analog circuits are fabricated using FinFET and triple-gate FETs. Digital circuit performance, leakage currents, and power dissipation are characterized. The triple-gate FET achieves the lowest gate delay (27ps at 1.2V) and is >30% faster than FinFET with same oxide thickness of 2nm and gate lengths of 80nm. A FinFET-based Miller OpAmp achieves 45dB dc gain at 1.5V.

23.3 A Low-Power True Random Number Generator Using the Random Telegraph Noise of Single Oxide-Traps **9:30 AM**
R. Brederlow, Infineon, Munich, Germany

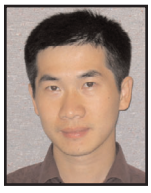
A true random number generator is realized by utilizing the noise produced by single oxide traps in small-area MOSFETs in combination with built-in redundancy. The circuit has an area of 0.009mm^2 in 0.12μm CMOS and consumes 50μW at 200kb/s random output data. The concept is robust against environmental noise and supply-voltage variations and is thus suitable for operation within security controllers.

23.4 A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link **10:15 AM**
N. Miura, Keio University, Yokohama, Japan

A 1Tb/s 3W inter-chip transceiver transmits clock and data by inductive coupling at a clock rate of 1GHz and data rate of 1Gb/s per channel. 1024 data transceivers are arranged with a pitch of 30μm. The total layout area is 2mm^2 in 0.18μm CMOS and the chip thickness is 10μm. 4-phase TDMA reduces crosstalk and the BER is <10^{-12}. Bi-phase modulation is used to improve noise immunity, reducing power in the transceiver.

23.5 Optical Interconnect Technologies for High-Speed VLSI Chips Using Silicon Nano-Photonics **10:45 AM**
K. Ohashi, NEC, Tsukuba, Japan

Optoelectronic and electrooptic elements are integrated on VLSI chips. The junction capacitance of a nano-photodiode is extremely low (<10aF), which permits a high load resistance to be used, resulting in higher output voltage at high frequencies. A ceramic Pb(,ZrTi)O_3 film with average crystallite diameter below 20nm has a high electro-optical coefficient (>150pm/V) suitable for on-chip modulators.



23.6 An Asynchronous Array of Simple Processors for DSP Applications **11:15 AM**
Z. Yu, University of California, Davis, CA

An array of simple programmable processors designed for DSP applications is implemented in 0.18μm CMOS and contains 36 asynchronously clocked independent processors. The processors operate at 475MHz, and each processor has a maximum power of 144mW at 1.8V and occupies 0.66 mm^2.

23.7 System-in-Silicon Architecture and its Application to an H.264/AVC Motion Estimate for 1080HDTV **11:45 AM**
K. Kumagai, System Fabrication Technologies, Yokohama, Japan

System-in-silicon (SiS) is a multi-chip architecture to realize wide bandwidth communication between logic and memory with low power. The application of SiS to H.264/AVC motion estimation is presented. DRAM is integrated with 23.1Gb/s bandwidth and 1.6pJ/b data transfer efficiency, realizing real-time 1080HDTV processing with 263.1GB/s.

23.8 A Chip-scale Electrical Soliton Modelocked Oscillator **12:00 PM**
D. Ricketts, Harvard University, Cambridge, MA

This paper introduces a chip-scale electrical soliton modelocked oscillator, which self-generates a periodic train of electrical soliton pulses. This circuit is made possible by combining a nonlinear transmission line (NLTL) with a unique amplifier that tames the instability-prone soliton dynamics in a closed-loop NLTL. This chip-scale prototype produces a pulse width of 293ps and demonstrates the feasibility for future widths close to 1ps, adding a new direction in pulse-based electronics.